



Venture Center  
100, NCL Innovation Park  
Dr. Homi Bhabha Road, Pune -411008  
Email: [eventsdesk@venturecenter.co.in](mailto:eventsdesk@venturecenter.co.in)  
Phone: +91-20250934

Technical Workshop Series

## 4-day Hands-on Workshop on **Multi-Core Computing** (Introduction to Pthreads , MPI , MMX & OpenCL)

<b>LEARN</b>	Introduction to Multi-Core Computing - Concepts, Multi-Core Architecture, Introductory Parallel Algorithms, Data and Task parallel Computing using Open Source Tools. Hands-on sessions.
<b>FOR WHOM</b>	<ul style="list-style-type: none"><li>• Aspiring Entrepreneurs in High Performance Computing</li><li>• Multi-Core learning aspirants with background in Computer Science</li><li>• Researchers in Signal Processing / Image Processing / Simulation</li><li>• PG students/ Final year UG students in electronics/ computer science engg</li></ul>
<b>WHEN</b>	Saturday, 4 <sup>th</sup> August 2012 Saturday, 11 <sup>th</sup> August 2012 Saturday, 18 <sup>th</sup> August 2012 Saturday, 25 <sup>th</sup> August 2012 Time: 2 PM – 7 PM
<b>WHERE</b>	E-Class Room, Venture Center (Entrepreneurship Development Centre) 100, NCL Innovation Park, National Chemical Laboratory Campus Dr Homi Bhabha Road/ Pashan Road, Pune - 411008
<b>CONTACT</b>	Administrative queries: Miss Lipika Biswas 100 NCL Innovation park, Dr. Homi Bhabha road, Pashan, Pune- 411008 Phone no- 20250934 Email:- <a href="mailto:eventsdesk@venturecenter.co.in">eventsdesk@venturecenter.co.in</a>  Technical queries: Mr S Basu; Phone: +73500-39098 ; +91-9260462088  For more information, visit: <a href="http://www.venturecenter.co.in/workshops/">http://www.venturecenter.co.in/workshops/</a>
<b>FEE</b>	Rs 7000 per person for all 4 days. Group Discount of 25% for groups of 5 or more <b>Limited seats. First-come-first-serve</b>



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### Workshop Description

Multi-Core processors have been making foray into our daily lives. Most laptops today are Dual Core and most Desktops Quad Core. As per product planning of the major chip makers, the core numbers would only grow. The Application makers and the users of such systems have been provided with an opportunity but they need the right language and the right tool to take advantage of such a system.

The Workshop focuses on:

- **x86 Multi-Core Architecture:** x86 is the most popular architecture having a lions share of the server market. x86 vendors like Intel and AMD also create Multi-core designs every quarter. Here we take a peek at the internals to understand why a certain processor is better than the other, what features are there which we can utilize through Multi-Core programming.
- **Introduction to Parallel Computing:** We take an algorithmic view of programming Multi-Core processors, comparing serial code executing with parallel code execution. We also warn the programmers about synchronization, deadlocks and other pitfalls with parallel execution. We look at the parallel coding granularity so that the best tool for the execution can be selected.
- **Task Parallel Computing:** If the granularity of the parallel task to be performed is relatively large and can be broken into separate tasks either similar or otherwise then they fall into the category of Task Parallel Computing. Threading is a large granularity Task Parallel Computing method, which is the only type present in legacy code which can take benefit of Multi-Cores. However when we wish to move towards large number tasks, Threading is no longer useful which is where MPI comes into play.
- **Data Parallel Computing:** When our computing needs are of SIMD nature i.e. we wish to execute similar code for a large number of data, MMX (Multi Media eXtensions) instructions of x86 help us out. When the data type is humongous we need to look beyond the CPU . OpenCL is a computing API which helps in coding such problems which run in either CPU or GPU.
- **Hands on programming:** Our Workshop also includes hands-on programming on the languages and tools to accelerate learning . This is the major focus of the workshop.
- **Tools Installation:** We also help attendees set-up their laptops (Linux Preferred ) so that they are enabled to participate in the workshop.

We would be using AMD CPU's and GPU's for the Hands-On session, lent to us by AMD, India.

More resources can be found at

<http://developer.amd.com/india>

OpenCL reference can be found at the site as well as Information for the OpenCL Book **“Heterogeneous Computing with OpenCL”** by Benedict Gaster, Lee Howes, David R. Kaeli, Perhaad Mistry & Dana Schaa.



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## Synopsis

- x86 Multi\_core Architecture
  - Multicore Processor
  - Inter-processor connectivity
  - Cache Architecture
  - Shared memory Architecture
- Introduction to Parallel computing
  - Serial vs Parallel Algorithms
  - Parallel Tasks granularity
- Task Parallel Computing
  - pthreads
  - MPI
- Data parallel Computing
  - MMX & SSE
  - OpenCL (Using AMD API)

## Target audience

- Aspiring Entrepreneurs in High Performance Computing
- Multi-Core learning aspirants with background in Computer Science
- Researchers in SignalProcessing / Image Processing / Simulation
- PG students/ Final year UG students in electronics/ computer science engg
- **Note:**  
Participants need to have studied or taken basic courses in C, Linux, Computing Basics  
Participants need a Laptop

## Faculty

The workshop shall be taught by Mr **S. Basu**.

**Profile :** Design Engineer with experience in both Digital and Analog Design. Experienced in a multitude of EDA and simulation tools. Strong interests in Embedded systems design and multicore code design. Hobby Robotics fan and entrepreneur in related field.

**Education :** B.Tech (H) '03 , M.Tech '04 (Indian Institute Of Technology , Kharagpur)

**Experience:** Component Design Engineer for Intel India's first Multicore project; Co-author of Enhanced Structural Tester Based Functional Test methodology for Intel Multicore processors; Mixed-Signal Design Consultant for National Semiconductor's Sponsored Project at IIT Kharagpur; Entrepreneur and Design Engineer

**Research and previous Workshops:** Behavioral Modelling for Mixed Signal Sytems using Verilog-AMS speeding up simulation times by 1000x; Analysis of spice simulation engine for simulation speedup; Computer Architecture : Multi-core programming using Message Passing Interface and CUDA; Workshop on Behavioral Modelling at IIT Kharagpur; Workshop on SPICE at College of Engg, Pune; Workshop on Digital Design at Venture Center, Pune.



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## Schedule

Timings	Topic	Duration	Comments
<b>DAY 1:</b>			
14:00 - 15:00	Introduction	60 mins	Introduction to Multi-Core Architecture
	Hardware Design Evolution		
	Current Trends		
	Block Diagram of a Single Core processor		
15:00 - 15:15	Break	15 mins	
15:15 - 16:30	Single Core to Multi-Core	75 mins	Multi-Core Internals
	Inter Processor Connectivity		
	Cache Architecture		
	Shared Memory Architecture		
16:30 -17:00	Snacks	30 mins	
17:00 - 18:00	Tools Setup	60 mins	Tools Setup
	Task parallel Computing		Introduction into Task parallel computing
	pthread Library overview		
18:00 -18:15	Break	15 mins	
18:15 - 19:00	Tutorial : Synchronization	45 mins	Hands-On pThreads
	Tutorial : Matrix Multiplication		
<b>DAY 2 :</b>			
14:00 - 15:00	Quick-Review	60 mins	Introduction to Parallel Algorithms
	Formal Machine Topologies		
15:00 - 15:15	Break	15 mins	
15:15 - 16:30	Interconnect Architecture	75 mins	Parallel Algorithms Continued
	Order of computation		
	Semaphores		
	Message Passing		
	Remote Procedure Calls		
	Speedup		
	Parallel Algorithm Examples		
16:30 -17:00	Snacks	30 mins	
17:00 - 18:00	Tools Setup	60 mins	Tools Setup
	Task parallel Computing :MPI		Introduction into Task parallel computing



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	MPI Library overview		
18:00 -18:15	Break	15 mins	
18:15 – 19:00	Tutorial : Scan-Reduce	45 mins	Hands-On MPI
	Tutorial : Matrix Multiplication		
<b>DAY 3 :</b>			
14:00 - 15:00	Quick-Review	60 mins	Introduction to Data Parallel Computing
	Backlog Clear		
15:00 - 15:15	Break	15 mins	
15:15 - 16:30	What is MMX	75 mins	Pentium MMX Architecture
	SIMD Basics		
	MMX instruction set overview		
	SSE Instruction set overview		
	Tutorial : Matrix Multiplication		
16:30 -17:00	Snacks	30 mins	
17:00 - 18:00	Bringing it All Together : OpenCL	60 mins	Introduction to OpenCL
	Platform Model		
	Memory Model		
	Programming Model		
18:00 -18:15	Break	15 mins	
18:15 – 19:00	OpenCL runtime	45 mins	OpenCL -Continued
	Tools Setup		
<b>DAY 4 :</b>			
14:00 - 15:00	Quick-Review	60 mins	Introduction to OpenCL
	Tools Setup		
15:00 - 15:15	Break	15 mins	
15:15 - 16:30	OpenCL Library	75 mins	OpenCL programming
	OpenCL variable types		
	Tutorial : Reduction		
	Tutorial : Matrix Multiplication		
16:30 -17:00	Snacks	30 mins	
17:00 - 18:00	Comparison of various platforms	60 mins	Performance Stats
18:00 -18:15	Break	15 mins	
18:15 – 19:00	Q&A	45 mins	Closure
	Certificate Distribution		



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### Workshop includes

- Classroom and practical sessions about Multi-Core Computing and get practical insights
- 200 page handout with useful, practical information
- Access to a restricted website with links to useful resources, software resources etc
- Joining a mailing list community of High Performance Computing enthusiasts
- Certificate of Participation from Venture Center
- Tea/Coffee/Snacks at Venture Center Cafeteria

### About the organizers

Venture Center strives to nucleate and nurture technology and knowledge-based enterprises by leveraging the scientific and engineering competencies of the institutions in the "Pune region" in India. The Venture Center is a technology business incubator specializing in technology startups offering products and services exploiting scientific expertise in the areas of materials, chemicals and biological sciences & engineering. The Venture Center is the trademark of Entrepreneurship Development Center, a not-for-profit company hosted by the National Chemical Laboratory, Pune, India.

More information is available at: <http://www.venturecenter.co.in/>